

Description

[DRAM STRUCTURE AND FABRICATING METHOD THEREOF]

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the priority benefit of Taiwan application serial no.92125866, filed on September 19, 2003.

BACKGROUND OF INVENTION

[0002] Field of the Invention

[0003] The present invention relates to a semiconductor fabrication process. More particularly, the present invention relates to a method of fabricating a dynamic random access memory (DRAM).

[0004] Description of the Related Art

[0005] Dynamic random access memory (DRAM) is a type of non-volatile and easy-to-access memory mostly for holding operating data in a computer. Typically, a DRAM consists of an array of cells each comprising a metal-ox-

ide-semiconductor (MOS) transistor and a capacitor. The source/drain regions of the transistor are electrically connected to a capacitor and a bit line respectively. At present, DRAM capacitors are classified into stacked capacitor or trench capacitor. A stacked capacitor is formed over the transistor and a trench capacitor is formed below the transistor.

[0006] To lower the sub-threshold current of the transistor and increase data retention capacity of storage electrode in a trench type DRAM capacitor, dosage level of the threshold voltage adjustment implantation and/or pocket implantation is often increased. The pocket implantation is a process of forming a doped pocket region on one side of a bit line connected source/drain region. However, this process also intensifies the rise in electric field at the PN junction and hence increases the leakage current there.

SUMMARY OF INVENTION

[0007] Accordingly, at least one object of the present invention is to provide a dynamic random access memory (DRAM) fabrication process. In the process, a doped region having the same conductive type as a substrate is formed in a section of a channel close to an isolation region to reduce sub-threshold current.

[0008] To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the invention provides a method of fabricating a dynamic random access memory (DRAM). First, trenches are formed in a substrate. A capacitor is formed inside each trench. Thereafter, active regions are defined over the substrate and then word lines are formed over the substrate. A pair of source/drain regions is formed in each active region and then bit lines are formed over the substrate. A first side of each active region has a first trench. The capacitor is coupled to the active region. Furthermore, a second side of each active region has a second trench. The word line passes through the active region and the second trench. The area in the active region covered by the word line serves as a channel region. In addition, the pair of source/drain regions in each active region is located on each side of a corresponding word line. The source/drain regions are electrically connected to a capacitor and a bit line respectively. One major aspect of this invention is the performance of a tilt ion implantation along the direction of the word line after forming the trenches but before defining the active regions. As a result, a doped region having the same conductive type as

the substrate is formed on the edge of a region for forming the channel.

[0009] This invention also provides a dynamic random access memory (DRAM) structure fabricated using the aforementioned DRAM fabrication process. One major aspect of the DRAM structure is the presence of a doped region on a side edge of the channel region away from the source/drain region. The doped region has a conductive type identical to the substrate and a range limited to within the channel region.

[0010] In this invention, a word line passes over the trench adjacent to the second side edge of the active region. Furthermore, the doped region is formed on the side edge of the active region through a tilt ion implantation via the trench. Hence, the doped region is formed in a self-aligned manner in a section of the channel adjacent to an isolation region. Because the concentration of dopants in the doped region is higher, sub-threshold current in the channel region is suppressed. Furthermore, by increasing the depth of the doped region, punch-through leakage can be reduced.

[0011] It is to be understood that both the foregoing general description and the following detailed description are exem-

plary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF DRAWINGS

[0012] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0013] Figs. 1 through 8 are diagrams showing the steps for producing a DRAM structure according to one preferred embodiment of this invention. In Figs. 1, 2 and 7, the sub-diagrams with a label (C) are top views and the sub-diagrams with a label (A)/(B) are cross-sectional views along line A-A"/B-B" of the one labeled (C). In addition, Figs. 7 and 8 are also diagrams for showing the DRAM structure according to one preferred embodiment of this invention.

DETAILED DESCRIPTION

[0014] Reference will now be made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever

possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

[0015] Figs. 1 through 8 are diagrams showing the steps for producing a DRAM structure according to one preferred embodiment of this invention. In Figs. 1, 2 and 7, the sub-diagrams with a label (C) are top views and the sub-diagrams with a label (A)/(B) are cross-sectional views along line A-A'/B-B' of the one labeled (C). As shown in Fig. 1(A)/(B)/(C), a substrate 100 such as a P-type monocrystalline silicon substrate is provided. Thereafter, a pad oxide layer 102 and a hard mask layer 104 are formed over the substrate 100. The hard mask layer 106 is a silicon nitride layer, for example. The hard mask layer 104, the pad oxide layer 102 and the substrate 100 are sequentially patterned to form a plurality of trenches 110 in the substrate 100. The trenches 110 are configured to form an eight F-square folded bit line DRAM layout detailed in U.S. Patent No. 5,874,758. In the eight F-square folded bit line DRAM layout, each area for forming an active region 130 is enclosed by four pairs of trenches 110 and each pair of trenches 110 is also enclosed by four areas for forming active regions 130. In addition, each area

for forming an active region 130 has a pair of trenches in the Y direction located underneath a subsequently formed word line 134.

[0016] As shown in Fig. 1(A)/(B), a doped region serving as an external electrode 112 is formed in the substrate 100 at a lower section of the trench 110. A capacitor dielectric layer 114 is formed on the surface of the trench 110. Conductive material is deposited into the lower section of the trenches to form conductive layers 116. Thereafter, the capacitor dielectric layer 114 not covered by the conductive layer 116 is removed. The dopants inside the external electrode 112 include arsenic (As) and the capacitor dielectric layer 114 is an oxide/nitride/oxide (ONO) composite layer or a nitride/oxide (NO) composite layer, for example. The conductive layer 116 serves as an inner electrode for a capacitor. In general, the conductive layer 116 is fabricated using N-type polysilicon, for example. The conductive layer 116 within the lower section of the trenches 110 is formed, for example, by depositing a conductive material to fill the trenches 110 entirely and then etching back the conductive material. In addition, the dash lines with a label 128 show a profile of a subsequently formed isolation region 128.

[0017] As shown in Fig. 2(A)/(B)/(C), a conformal dielectric layer 118 is formed over the substrate. The conformal dielectric layer 118 is, for example, a silicon oxide layer formed by performing a chemical vapor deposition using ozone (O₃) and tetra-ethyl-ortho-silicate (TEOS) as reactive gases. The dielectric layer 118 is a precursor to a subsequently formed collar dielectric layer. Thereafter, a tilt ion implantation 120 is carried out at a tilt angle along the Y direction through the upper section of the trenches 110. Ultimately, doped regions 122 are formed on the side edges of the active region 130 adjacent to the isolation region 128. The doped regions 122 have a conductive type identical to the substrate 100. Preferably, the concentration of dopants inside the doped regions 122 is between 1×10^{16} to 5×10^{18} . Because the pair of trenches 110 in the Y direction in Fig. 2(A) is located under two subsequently formed word lines 134 and the word line covered portion of the active region 130 are channel regions, the doped regions 122 are formed in a self-aligned manner. That is, the doped regions 122 are automatically formed in the substrate 100 on each side of the active region, on which predetermined channel region will be formed, adjacent to the isolation region 128 after the tilt ion implantation.

[0018] As shown in Fig. 3(A)/(B), the dielectric layer 118 above the conductive layer 116 and the hard mask layer 104 are removed and then another conductive material is deposited into the trenches 110 to form conductive layers 124 that expose a portion of the dielectric layer 118. The conductive layer 116 is an N-type polysilicon layer, for example. Thereafter, the dielectric layers 118 above than the conductive layers 124 are removed to form collar dielectric layers 118a.

[0019] As shown in Fig. 4(A)/(B), another conductive material is deposited into the trenches 110 to form conductive layers 126 with a top surface below the top surface of the substrate 100. The conductive material is N-type polysilicon, for example. The conductive layers 126 serves as an electrical connection between the inner electrode 116 and the source/drain region of a subsequently formed access transistor.

[0020] Although the aforementioned tilt ion implantation is carried out after forming the dielectric layer 118, the implantation to form doped regions 522 can alternatively be processed after forming the conductive layers 126. The implantation is shown in Fig. 5(A)/(B) by an arrow with a label 520. Because the trenches 110 are almost com-

pletely filled by now, the doped regions 522 have an implantation depth smaller than the aforementioned doped regions 122.

[0021] As shown in Fig. 6(A)/(B), an isolation region 128 is formed in the substrate 100 to pattern the active regions 130. Since the position of the isolation region 128 relative to the trenches 110 has been explained before, detailed description is not repeated. As shown in Fig. 6(A), the doped region 122 for lowering sub-threshold current is formed in the active regions 130 close to the isolation region 128. The isolation region 128 is a shallow trench isolation (STI) structure fabricated using silicon oxide material, for example. In the process of fabricating the isolation region 128, thermal treatment is often required. During the thermal treatment, some dopants within the conductive layers 126 also diffuse into the substrate 100 to form a buried strap 129 as shown in Fig. 6(B).

[0022] As shown in Fig. 7(A)/(B)/(C), a gate dielectric layer 132 is formed over the substrate 100 and then a plurality of word lines 134 with a cap layer 136 thereon is formed over the gate dielectric layer 132. The word lines 134 cover parts of the active region 130, serving as channel regions, and the doped regions 122 thereon. Thereafter,

using the cap layers 136 and the word lines 134 as a mask, an ion implantation 140 is performed to form source/drain regions 142. The source/drain region 142 between two word lines 134 above the same active region 130 is a common source/drain region. Meanwhile, each source/drain region 142 on the side edge of the active region 130 is connected to a buried strap 129 for connecting with a corresponding inner electrode 116. Thereafter, spacers 138 are formed on the sidewalls of the cap layers 136 and the word lines 134. The cap layers 136 and the spacers 138 are fabricated using silicon nitride material, for example. The cap layers 136 and the spacers 138 enclose and prevent the word lines 134 from being exposed during a subsequent bit line contact processing operation.

[0023] As shown in Fig. 8(A)/(B), an insulation layer 144 is formed over the substrate 100 covering various aforementioned structures. Thereafter, bit line contacts 146 are formed within the insulation layer 144 and then bit lines 148 are formed over the insulation layer 144 in contact with various bit line contacts 146. Because the top and side surface of each word line 134 are protected through the cap layer 136 and sidewall spacers 138, the bit line contacts 146 are formed in a self-aligned process.

[0024] In addition, Figs. 7 and 8 are also sectional views of a DRAM structure according to one preferred embodiment of this invention. The DRAM has a conventional eight F-square folded bit line buried strap structure. However, doped regions 122 are also incorporated in the design in this invention. The doped region 122 has a conductive type identical to the substrate 100. The DRAM structure comprises a substrate 100, active regions 130 surrounded by an isolation region 128, trenches 110, word lines 134, (common) source/drain regions 142, contacts 146, bit lines 148 and doped regions 122. The substrate 100 has a plurality of trenches 110. Each trench 110 encloses a capacitor comprising an external electrode 112, a capacitor dielectric layer 114 and an inner electrode 116. A pair of trenches 110 is position on all four sides of each active region 130. Among the pairs of trenches 110 on the left and right side of the active region 130, the capacitor inside one of the trenches 110 is electrically coupled to the active region 130. Furthermore, among the pairs of trenches 110 on the front and back sides of the active region 130, the capacitors inside the trenches 110 are electrically coupled to other active regions 130 (refer to Fig. 1). In addition, a pair of neighboring word lines 134

passes through the active region 130 as well as the pair of front and back trenches 110. The word lines 134 run in a first direction. The areas within the active region 130 covered by the pair of word lines 134 form two channel regions. The doped regions 122 are formed on the two sides of each channel region adjacent to the isolation region 128. The active region 130 between the two word lines 134 has a common source/drain region 142 electrically connected to the bit line 148 running in a second direction. The active region 130 also has two source/drain regions 142 on the outer edge of the two word lines 134 with each source/drain region 142 electrically connected to a corresponding capacitor.

[0025] As shown in Fig. 7(C), doped regions 122 having a conductive type identical to the substrate 100 are formed on each side of the channel region (the section in the active region 130 covered by the word lines 134) close to the isolation region 128. Therefore, sub-threshold current in the channel region is suppressed. Furthermore, if the depth of the doped region 122 is increased, even punch-through leakage can be minimized. For example, the doped region 122 formed after the dielectric layer 118 has a depth greater than the doped region 522 (shown in

Fig. 5(A)) formed after the conductive layer 126. Consequently, the doped region 122 is better able to resist any punch-through leakage.

[0026] The tilt ion implantation (Fig. 2(A)) is preferably carried out after forming the dielectric layer 118 (Fig. 2(A))(precursor to the collar dielectric layer) or after depositing the conductive material to form the topmost conductive layer 126 in the trenches 110 (Fig. 5(B)). However, the implantation can be carried out any time after forming the trenches 110 but before patterning the active regions 130. The only criteria is that the implantation must be carried out at a proper energy level and a proper tilt angle so that dopants can penetrate into the area on the side edges of the channel.

[0027] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.